| Tsuyama College                       |   | Year | 2020 |                  | Course<br>Title | Mathematical Information |  |  |
|---------------------------------------|---|------|------|------------------|-----------------|--------------------------|--|--|
| Course Information                    |   |      |      |                  |                 |                          |  |  |
| Course Code                           | urse Code 0085  |      |      |                  | Specializ       | Specialized / Compulsory |  |  |
| Class Format                          | Lecture   |      |      | Credits          | Academi         | Academic Credit: 2       |  |  |
| Department                            | Department of Integrated Science and<br>Technology Communication and<br>Informations System Program |      |      | Student Grade    | 4th             | 4th                      |  |  |
| Term                                  | Second Semester   |      |      | Classes per Week | 2               | 2                        |  |  |
| Textbook and/or<br>Teaching Materials |   |      |      |                  |                 |                          |  |  |
| Instructor                            | KAWANAMI Hiromichi  |      |      |                  |                 |                          |  |  |
| Course Objectives                     |   |      |      |                  |                 |                          |  |  |

Learning purposes: Understand principles of digital data processing, and design fundamental circuits for data processing.

- Course objectices:
  1. To design combinational circuits.
  2. To explain operations and characteristics of fundamental elements of a sequential circuits.
  3. To explain operations of fundamental sequential circuits.

## Rubric

| Rabite        |   |  |   |  |  |  |  |
|---------------|---|--|---|--|--|--|--|
|               | Excellent   | Good   | Acceptable  | Not acceptable                                       |  |  |  |
| Achievement 1 | The student can design desired combinational circuits.                | The student can design fundamental combinational circuits such as an adder.                                      | The student can design simple combinational circuits.   | The student does not reach the the acceptable level. |  |  |  |
| Achievement 2 | The student can exchange every flip-flop to equivalent flip-flops.    | The stundent can cleary explain operations and characteristics of fundamental elements of a sequential circuits. | The stundent can explain operations and characteristics of fundamental elements of a sequential circuits. | The student does not reach the the acceptable level. |  |  |  |
| Achievement 3 | The student can analyze and explain on arbitrary sequential circuits. | The student can analyze and clearly explain on fundamental sequential circuits.                                  | The student can analyze and explain fundamental sequential circuits.                                      | The student does not reach the the acceptable level. |  |  |  |

## Assigned Department Objectives

| Assigned Department Objectives |   |  |  |  |  |  |  |  |
|--------------------------------|---|--|--|--|--|--|--|--|
| Teaching Method                | Teaching Method   |  |  |  |  |  |  |  |
| Outline                        | General or Specialized: Specialized Field of learning: Information system, Programming, Networks Required, Elective, etc.: Must complete subjects Foundational academic disciplines: Informatics/Computing Technology/Computer System  Relationship with Educational Objectives: This class is equicalent to "(3) Acquire deep foundation knowledge of the major subject area".  Relationship with JABEE programs: The main goal of learning / education in this class are "A", "A-1", also "A-2" is involved.  Course outline: In this class, the students study loigic theory further, using examples of optimization design of combinational circuits and sequential circuits of logic circuits. |  |  |  |  |  |  |  |
| Style                          | Course method: This class is conducted mainly using the blackboard. To deepen understanding of contents the students work on exercises.  Grade evaluation method: Exams (75%) + Exercises (25%). Two regular examinations will be conducted 2 times, equally weighted. If necessary, a supplementary examination will be conducted. However, the updated evaluation will not exceed 60 points.  |  |  |  |  |  |  |  |
|                                | Precautions on the enrollment: Students must take this class (no more than one-thirds of the required number of class hours missed) in order to complete the 4th-grade course.  Course advice: Precisely understand meaning and definition of technical terms appeared in the textbook. It is also important to try example questions and exercises in every chapter and deeply understand them.  |  |  |  |  |  |  |  |
| Notice                         | Fundamental subjects: Information Literacy (1st year), Digital Circuits (2nd), Basic Programming (2nd), Digital Engineering (3rd), Applied Digital Circuits (3rd) Related subjects: Information Theory (5th year, Network), System Programming (5th), e-Business (5th), Information System Analysis (5th)   |  |  |  |  |  |  |  |

| Course I | Plan           |     |                       |   |
|----------|----------------|-----|-----------------------|---|
|          |                |     | Theme                 | Goals   |
|          | 3rd<br>Ouarter | 1st | IGUIDANCE DINALV CODE | Can operate fundamental arithmetric operation by binary code. |

Attendence advice : Listening to the lecture carefully is very important and the most effective way to understand. If you are late for the start time, your absence will be counted on every half class hour.

| 3r                          |   | 2nd         | Logic operation (1) (login function)  |  |               | Can explain conception of combinational circuits and logic function.                 |  |       |  |
|-----------------------------|---|-------------|---|--|---------------|--|--|-------|--|
|                             |   | 3rd         | Logic operation (2) (canonical forms)   |  |               | Can form a disjunctive canonical form and a conjunctive canonical form).             |  |       |  |
|                             |   | 4th         | Design of combinational circuirs (1).<br>(simplification using Karnaugh map)        |  |               | Can simplify combinational circuits using Boolean algebra and Karnaugh map.          |  |       |  |
|                             | 5th D                                       |             | Desing of combinational circuits (2).<br>(simplification using QM algorithm)        |  |               | Can simplify combinational circuits using Quine–McCluskey algorithm.                 |  |       |  |
|                             |   |             | Design of combinational circuits (3).<br>(Simplification for multi-output circuits) |  |               | Can simplify multiple-output combinational circuits using Quine–McCluskey algorithm. |  |       |  |
|                             | Major combinational circuits (addor decoder |             |   | Can explain fundamental combinational circuits.    |               |  |  |       |  |
|                             |   |             |   |  |               |  |  |       |  |
|                             |   | 9th         | Return and commentary of exam answers.  |  |               |  |  |       |  |
|                             |   |             | Flip-flop (1). (characteristics table, exitation table)                             |  |               | Can explain principles of fundamental operations of flip-flops.                      |  |       |  |
|                             |   | 11th        | Flip-flop (2). (mas   | Flip-flop (2). (mastar-slave FF, edge-triggerd FF) |               |  | Can explain principles of operations of advanced flip-flops. |       |  |
|                             | 4th   | 12th        | Fundamental sequential circuits. (non-synchronous / synchronous counter)            |  |               | Can design fundamental sequential circuits.  |  |       |  |
|                             | Quarte                                      | er<br>13th  |   |  |               | Can design applied sequential circuits.  |  |       |  |
|                             |   | 14th        | Practical sequenti vending machine)   |  | affic signai, | Can design practical sequential circuits.  |  |       |  |
|                             |   |             | Semester final exam.  |  |               |  |  |       |  |
|                             |   | 16th        | Return and comm   | Return and commentary of exam answers.             |               |  |  |       |  |
| Evaluati                    | on M  | ethod and   | Weight (%)  |  |               |  |  |       |  |
|                             |   | Examination | Presentation  | Mutual<br>Evaluations<br>between<br>students       | Behavior      | Exercise   | Other  | Total |  |
| Subtotal                    |   | 75          | 0   | 0  | 0             | 25   | 0  | 100   |  |
| Basic<br>Proficiency 0      |   | 0           | 0   | 0  | 0             | 0  | 0  | 0     |  |
| Specialized Proficiency 75  |   | 0           | 0   | 0  | 25            | 0  | 100  |       |  |
| Cross Area<br>Proficiency 0 |   | 0           | 0   | 0  | 0             | 0  | 0  |       |  |