| Akashi College  |  | ollege                        | Year 2023  |   |   |   | ourse<br>Title  | Advanced Electronic Circuit   |  |  |
|---|--|-------------------------------|--|---|---|---|---|---|--|--|
| Course  | Informa  | tion                          | <u> </u>   |   |   |   |   |   |  |  |
| Course Co   | ode  | 5035                          |  |   | Course Category   | tegory Specialized  |   | ed / Elective   |  |  |
| Class Format Lecture  |  |                               |  |   | Credits   |   | Academic Credit: 2  |   |  |  |
| Department Mechanica<br>Engineeri   |  |                               | cal and Electronic System<br>ina   |   | Student Grade   |   | Adv. 2nd  |   |  |  |
| Term First Sem  |  |                               |  |   | Classes per Week 2  |   | 2   |   |  |  |
| Textbook  |  |                               |  |   |   |   |   |   |  |  |
| Teaching<br>Instructor  |  | INOUE Ka                      | azunari  |   |   |   |   |   |  |  |
|   | Objectiv   |                               | azuriari   |   |   |   |   |   |  |  |
| This cours<br>understar<br>understar<br>have beer<br>technolog  | se will tead<br>nd the CMO<br>nd the road<br>n taken in  | ch VLSI devi<br>OS logic circ | uit, apply it to co  | imputer and contr   | ol circuits, learn t<br>more the aim is t   | the fea   | tures of v  | The objective is to correctly<br>various memory LSIs, and<br>he challenges and measures that<br>umption and reliability |  |  |
| Rubric  |  |                               |  |   | T   |   |   |   |  |  |
|   |  |                               | Ideal Level  |   | Standard Level  |   |   | Unacceptable Level  |  |  |
| Achievement 1   |  |                               | Fully understand circuit design and operation verification techniques.   |   | Understand circuit design and operation verification techniques.                            |   | sign and  | Do not understand circuit design and operation verification techniques.   |  |  |
| Achievement 2   |  |                               | Fully understand technologies for low power consumption and high speed.  |   | Understand technologies for low power consumption and high speed.                           |   | ies for lov<br>nd high  | Do not understand technologies for low power consumption and high speed.  |  |  |
| Achievement 3   |  |                               | Fully understand high-density<br>memory circuit technologies<br>such as SRAM, DRAM, and<br>Flash.  |   | Understand high-density<br>memory circuit technologies<br>such as SRAM, DRAM, and<br>Flash. |   | ologies   | Do not understand high-density<br>memory circuit technologies<br>such as SRAM, DRAM, and<br>Flash.                      |  |  |
| Assigne   | d Depar  | tment Ob                      | jectives   |   |   |   |   |   |  |  |
| Teachin   | g Metho  | od                            |  |   |   |   |   |   |  |  |
| Outline   | VLSI devices have achieved remarkable development in three key areas: higher speed, lower power consumption, and higher integration. The course will lecture on circuit and architecture technologies regardi high-performance design techniques for achieving them.  In this course, lessons will be conducted in a lecture style format. Students will be introduced to the high-performance design electronic circuits of recent years by faculty members with practical experience in memory and application processor design. |                               |  |   |   |   |   |   |  |  |
| Classes will be taught in lecture and exercise formats for the following numbers 1) to 3). The exams, and evaluation will be based on the submitted assignment.  1) Understand circuit design and operational verification technologies. 2) Understand technologies for low power consumption and high speed. 3) Understand high-density memory circuit technologies such as SRAM, DRAM, and Flash. |  |                               |  |   |   |   |   |   |  |  |
| Notice  |  | This cour<br>guarante         | rese's content will amount to 90 hours of study in total. These hours include the learning time eed in classes and the standard self-study time required for pre-study / review, and completing ent reports.  S who miss 1/3 or more of classes will not be eligible for evaluation. |   |   |   |   |   |  |  |
| Charact   | eristics (   |                               | Division in Le   |   | Will flot be eligible   | 101 6   | raidation.  |   |  |  |
|   |  | or Class /                    |  |   |   | to Romato Class   |   |   |  |  |
| ☐ Active  | Learning   |                               | ☑ Aided by IO  | Applicable to Remote Class Experienced  |   |   |   |   |  |  |
| _   |  |                               |  |   |   |   |   |   |  |  |
| Course  | Plan   | Ι Ι-                          | TI   |   |   | CI-   |   |   |  |  |
| 1st<br>Semeste<br>r   | 1st<br>Quarter   | 1st                           | Theme  Lecture overview and trends toward higher performance VLSI  Explain the lecture overview for Advanced Electronic Circuits.  |   |   | Goals  Lecture overview and trends toward higher performance VLSI Understand the lecture overview for Advanced Electronic Circuits. |   |   |  |  |
|   |  | 2nd r                         | nMOS/pMOS trar   | nsistors and CMOS<br>MOS transistor and   | inverters r<br>CMOS inverter  | nMOS/pMOS transistors and CMOS inverters<br>Understand nMOS/pMOS transistor and CMOS<br>inverter operation.                         |   |   |  |  |
|   |  | 2rd (                         | CMOS logic circu   | MOS logic circuits chair the various CMOS logic circuits.   |   |   | CMOS logic circuits<br>Understand CMOS logic circuits.  |   |  |  |
|   |  | 4th E                         | Explain the comb   | ombinational circuits using CMOS<br>cplain the combinational circuits that are<br>imposed of CMOS logic circuits. |   |   | Combinational circuits using CMOS<br>Understand the combinational circuits that are<br>composed of CMOS logic circuits.     |   |  |  |
|   |  | 5th E                         | CMOS-based seq   | based sequential circuits<br>the sequential circuits that are composed  |   |   | CMOS-based sequential circuits Understand the sequential circuits that are composed of CMOS logic circuits.                 |   |  |  |
|   |  | 6th                           | _SI manufacturir<br>Explain topics su  |   |   |   | LSI manufacturing process<br>Understand topics such as silicon substrates, gate<br>oxide film formation, and ion injection. |   |  |  |
|   |  | 7th                           | /LSI design<br>Explain functiona   | al design, hardwar<br>rification in LSI de  | e description   | VLSI design Understand functional design, hardware description language and verification in LSI design.                             |   |   |  |  |
|   |  |                               |  | tile memory circuits<br>ain SRAM and DRAM circuit configuration and<br>ation.                                     |   |   | Volatile memory circuits Understand SRAM and DRAM circuit configuration and operation.                                      |   |  |  |

|                                  | 2nd<br>Quarter | 9th        | Non-volatile memore Explain non-volatily and operation.  |                   | configuration | Non-volatile memory circuits Understand non-volatile memory circuit configuration and operation.  |   |       |  |  |
|----------------------------------|----------------|------------|--|-------------------|---------------|---|---|-------|--|--|
|                                  |                | 10th       | Circuit design exercises using SPICE 1 Explain circuit inputs using SPICE.   |                   |               | Circuit design exercises using SPICE 1<br>Understand circuit inputs using SPICE.  |   |       |  |  |
|                                  |                | 11th       | Circuit design exercises using SPICE 2 Explain circuit inputs and operation verification using SPICE.  |                   |               | Circuit design exercises using SPICE 2<br>Understand circuit inputs and operation<br>verification using SPICE .                               |   |       |  |  |
|                                  |                | 12th       | Circuit design usin<br>submission 1<br>Solve the problem<br>operation verificat  | s regarding circu |               | Circuit design using SPICE; Assignment submission 1 Solve the problems regarding circuit inputs and operation verification using SPICE.       |   |       |  |  |
|                                  |                | 13th       | Circuit design using SPICE; Assignment submission 2 Solve and submit the problems regarding circuit inputs and operation verification using SPICE. |                   |               | Circuit design using SPICE; Assignment submission 2 Solve the problems regarding circuit inputs and operation verification using SPICE.       |   |       |  |  |
|                                  |                | 14th       | Testing and reliability design<br>Explain coverage and design for testability.   |                   |               | Testing and reliability design Understand coverage and design for testability.  |   |       |  |  |
|                                  |                | 15th       | Summary and future trends Explain topics such as more than Moore, IoT sensor nodes, and other future development trends in VLSI technology.        |                   |               | Summary and future trends Understand topics such as more than Moore, IoT sensor nodes and other future development trends in VLSI technology. |   |       |  |  |
|                                  |                | 16th       | No final exam  |                   |               |   |   |       |  |  |
| Evaluation Method and Weight (%) |                |            |  |                   |               |   |   |       |  |  |
|                                  |                | ssignments |  |                   |               |   |   | Total |  |  |
| Subtotal                         |                | 00         | 0  | 0                 | 0             | 0   | 0 | 100   |  |  |
| Basic<br>Proficiency             | 0              |            | 0  | 0                 | 0             | 0   | 0 | 0     |  |  |
| Specialized<br>Proficiency       |                | 00         | 0  | 0                 | 0             | 0   | 0 | 100   |  |  |
| Cross Area<br>Proficiency        |                |            | 0  | 0                 | 0             | 0   | 0 | 0     |  |  |