| Tsuyama College | | Year | ear 2022 | | | Course Title | Inform | nation System | | | | |
|---|--|---|-------------------------------------|---|-----------------|--|----------|--|--|--|--|--|
| Course Information | on | | | | | | | | | | | |
| Course Code | | Course Category | | Specialize | | npulsory | | | | | | |
| Class Format | Lecture | | | Credits | Academic Credit | | | 2 | | | | |
| Department | Technology | of Integrated s Communication s System Progr | n and | se and Student Grade | | 4th | | | | | | |
| Term | Second Sem | nester | | Classes per V | Week | 2 | | | | | | |
| Textbook and/or | Textbook: K | eitaro HORI, "Z | Zukai Computer / | Architecture N | uumo | n (Illustrated | Introdu | ction to Computer | | | | |
| Teaching Materials Instructor | Textbook: Keitaro HORI, "Zukai Computer Architecture Nuumon (Illustrated Introduction to Computer Architecture) 2nd Edition" (Morikita Shuppan) MORI Yoshiya | | | | | | | | | | | |
| | | /a | | | | | | | | | | |
| Course Objectives Learning purposes : L design philosophy and | earn structur | res and mechar the relationshi | nisms of compute p between hardv | er systems systems systems and softw | stema vare. | tically from t | ne stand | poin of architecture- | | | | |
| Course objectives : 1. To understand and 2. To understand and 3. To understand and | explain majo | or designs of Cl | PUs. | iter system. | | | | | | | | |
| Rubric | | | | | | | | | | | | |
| | Exceller | nt | Good | | Accei | ptable | | Not acceptable | | | | |
| Chievement 1 | | dent can ely explain es of major er systems anc vantages and | concretely e structures of | The student can concretely explain structures of major computer systems. | | The student can explain general structures of major computer systems. | | The student does not reach the the acceptable level. | | | | |
| Achievement 2 designs and the | | ntages. dent can ely explain of major CPUs ir advantages a ntages. | concretely e | The student can concretely explain designs of major CPUs. | | The student can concretely explain general designs of major CPUs. | | The student does not reach the the acceptable level. | | | | |
| Achievement 3 Achievement 3 | | dent can ely explain of major mem s and their ages and | ory concretely e | designs of major memory | | The student can concretely explain general designs of major memory systems. | | The student does not reach the the acceptable level. | | | | |
| Assigned Departn | nent Objec | ctives | | | | | | | | | | |
| Teaching Method | | | | | | | | | | | | |
| Outline | General or Specialized : Specialized Field of learning : Information systems, Programming, Networks Foundational academic disciplines : Informatcs/Computer System, Information Networks Relationship with Educational Objectives: This class is equicalent to "(3) Acquire deep foundation knowledge of the major subject area". Course outline : Deepen knowledge on a computer systems and learn structures and mechanisms of computer systems systematically from the standpoint of architecture design philosophy. | | | | | | | | | | | |
| Style | Course method : This class is conducted mainly using a blackboard. To deepen understanding of content, the students are expected to work on exercises. | | | | | | | | | | | |
| | Grade evaluation method : Two times regular exams (75%) + Exercises (25%). Regular examinations will be conducted 2 times, equally weighted. The final evaluation can be updated via supplementary examinations. | | | | | | | | | | | |
| | Precautions on the enrollment : Students must take this class (no more than one-thirds of the required number of class hours missed) in order to complete the 4th grade course. This is a class that requires study outside of class hours. A total of 45 hours of study is required per credit, including both class time and study outside class time. Follow the instructions of the instructor regarding study outside of class hours. | | | | | | | | | | | |
| Notice | Course advice : The contents of this class deeply relate to subjects on computer systems in the lower grades. | | | | | | | | | | | |
| | Fundamental subjects : Digital Engineering (3rd year), Applied Digital Circuits (3), Introduction to Computers (3), Mathemarical Information (4) Related subjects : Information System Analysis (5th year, Network), System Programming (5th) | | | | | | | | | | | |
| | Attendence advice : The studens are expected to understand technical terms appeared in the "Information-Technology Engineers Examination". If you try to study considering with your own PC , your understanding can be deepen. If you are late for the start time, your absence will be counted on every half class hour. | | | | | | | | | | | |
| Characteristics of | Class / Di | vision in Lea | arning | 1 | | | | | | | | |
| □ Active Learning □ Aided by ICT □ A | | | | | | emote Class | | structor Professionally ienced | | | | |

| Must | comp | lete s | subjects | | | | | | | |
|-------------------------------|----------------|------------|--|---|------------------|--|--|-------|--|--|
| Course | | | * | | | | | | | |
| | | | Theme | | Goals | | | | | |
| 2nd Semeste - r | 3rd Quarter | 1st | Guidance. History system. | Suidance. History and classification of a computer ystem. | | | Can explain the outline and the goal of this class. | | | |
| | | 2nd | Characteristics of von Neumann architecture. | | | Can explain the characteristics of a von Neumann architecture computer system. | | | | |
| | | 3rd | Instruction set (1) - Structure of an i - Structure set. | Structure of an instruction form. | | | Can explain a structure of an instruction set. | | | |
| | | 4th | nstruction set (2) Evaluation of machanism of an instruction. Addressing. | | | Can explain a mechanism of instruction and addressing. | | | | |
| | | 5th | CPU architecture - Harvard architecture. - RISC and CISC. | | | Can explain CPU architectures. | | | | |
| | | 6th | Control architecture (1) - Wired logic control system and its structure. | | | Can explain a wired logic controy system. | | | | |
| | | 7th | Control architectu - Micro-program c | re (2) control system an | d its structure. | Can explain a micro-program contol system. | | | | |
| | | 8th | Semester mid-ter | m exam | | | | | | |
| | 4th Quarter | 9th | Return and comm | entary of exam a | inswers | | | | | |
| | | 10th | Cache memory (1) - Mechanism of cache memory. - First and second level cache. | | | Can explain a mechanism of cache memory. | | | | |
| | | 11th | - Mapping method | Cache momory (2) Mapping method of cache memory Transmission method to main mamory. | | | Can explain a mapping system of cache momory. | | | |
| | | 12th | | /irtual memory (1) Mechanism of virtual memory. Paging method. | | | Can explain a paging method of virtual memory. | | | |
| | | 13th | Virtual memory (2 - Segmentation m - Mapping method | Segmentation méthod. | | | Can explain a segmentation method of virtual memory. | | | |
| | | 14th | nterrupt processing and pipeline processing Mechanism of interrupt processing Mechanism of pipeline processing | | | Can explain an interrupt processing and a pipeline processing. | | | | |
| | | 15th | Semester final exam | | | | | | | |
| | | 16th | Return and comm | entary of exam a | inswers | | | | | |
| Evaluat | ion Me | thod and N | Weight (%) | | 1 | | | | | |
| | E | xamination | Presentation | Mutual Evaluations between students | Behavior | Exercise | Other | Total | | |
| Subtotal 75 | | 0 | 0 | 0 | 25 | 0 | 100 | | | |
| Basic Proficiency 0 | | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| Specialized Proficiency 75 | | 5 | 0 | 0 | 0 | 25 | 0 | 100 | | |
| Cross Are Proficienc | | | 0 | 0 | 0 | 0 | 0 | 0 | | |